

Analysis & Design of Low Power CMOS Comparator at 90nm Technology

Shruti Hathwalia

Department of EECE ITM University, Gurgaon, Haryana

Abstract

High speed and low power comparators are the essential building blocks of high speed Analog to digital converters (ADCs). This paper provides a comprehensive review about a variety of comparator designs - in terms of performance, power and delay. Preamplifier dynamic latch circuit that consists of a preamplifier followed by a double regenerative dynamic latch, this preamplifier uses fully differential circuit which decreases the effects of offset voltage error due to device mismatch. Buffered dynamic latch circuit includes a basic dynamic latch comparator followed by an inverter buffer stage. The inverter buffers are added to isolate the comparator output and large node capacitance also used to minimize the offset errors. Comparators are designed and simulated their Transient responses in Cadence Virtuoso Analog Design Environment using GPDK 90nm technology.

I. INTRODUCTION

In today's world, where demand for portable battery operated devices is increasing, a major thrust is given towards low power methodologies for high speed applications. This reduction in power can be achieved by moving towards smaller feature size processes. However, as we move towards smaller feature size processes, the process variations and other non-idealities will greatly affect the overall performance of the device. One such application where low power dissipation, low noise, high speed, less Offset voltage are required is Analog to Digital converters for mobile and portable devices. [3] The performance limiting blocks in such ADCs are typically inter-stage gain amplifiers and comparators. The accuracy of such comparators, which is defined by its offset, along with power consumption, delay is of keen interest in achieving overall higher performance of ADCs. In the past, pre-amplifier based comparators have been used for ADC architectures such as flash and pipeline. [5] The main drawback of pre-amplifier based comparators is the more offset voltage. To overcome this problem, dynamic comparators are often used that make a comparison once every clock period and require much less offset voltage. However, these dynamic comparators suffer from large power dissipation compared to pre-amplifier based comparators. The basic component in ADC device is a comparator. The basic comparator consists of three blocks as shown in Figure 1 below:

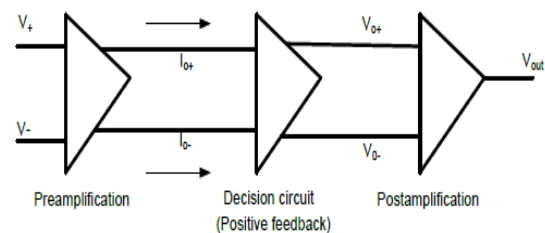


Figure 1. Block diagram of Comparator [2]

II. BACKGROUND

Among the circuits proposed in literature, some are concerned with speed [4], some may be emphasizing on low power and high resolution, and some on offset cancellation. In our work, we studied the various proposed literatures and designed an improved one with a view to reduce the comparator size and make it adaptable for high speed.

Heung Jun Jeon *et al.* [4] investigated that a novel dynamic latched comparator has lower offset voltage and higher load drivability than the conventional dynamic latched comparators. With two additional inverters inserted between the input- and output-stage of the conventional double-tail dynamic comparator, the gain preceding the regenerative latch stage is improved. The complementary version of the regenerative latch stage, which provides larger output drive current than the conventional one at a limited area, is implemented.

Bang-Sup Song [10] proposed a comparator circuit with only preamplifier and decision stage, but did not provide any experimental results to analyze the circuit performance.

Amalan Nag [11] proposed a comparator with 200 MHz speed and with offset cancellation. We had taken his idea and continued our project by focusing on the speed of the circuit.

III. CIRCUIT DESCRIPTION

A. Conventional Three stage CMOS Comparator

i. Pre-amplification : [5]

For the preamplifier stage, the circuit is as shown in Figure 2. The circuit is a differential amplifier with active loads. The size of M1 and M2 are set by considering the differential amplifier's transconductance and the input capacitance. The transconductance sets the gain of the stages, while the input capacitance of the comparator is determined by the size M1 and M2. We have concentrated on speed in this design, and hence no high impedance nodes are used in the circuit, other than the input and output nodes.

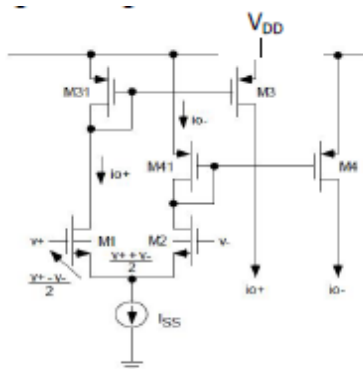


Figure 2. Pre-Amplifier [3]

ii. Decision Circuit: [2]

The decision circuit is the heart of the comparator and it should be capable of discriminating signals around 10 mV. The circuit used in our design is shown in Figure 3. The circuit uses positive feedback from the cross gate connection of M6 and M7 to increase the gain of the decision element.

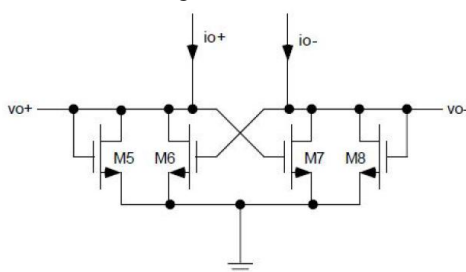


Figure 3. Decision Circuit [3]

iii. Output Buffer:[3]

The final component in our comparator design is the output buffer or post-amplifier, which is shown in Figure 4. The main purpose of the output buffer is to convert the output of the decision circuit

into a logic signal i.e. either a 0(-VDD) or 1(VDD). The output buffer should accept a differential input signal and not have slew rate limitations. The output buffer used in conventional comparator design is shown in Figure 4. This is a self biasing differential amplifier. An inverter was added at the output of the amplifier as an additional gain stage, to isolate any load capacitance from the self biasing differential amplifier.

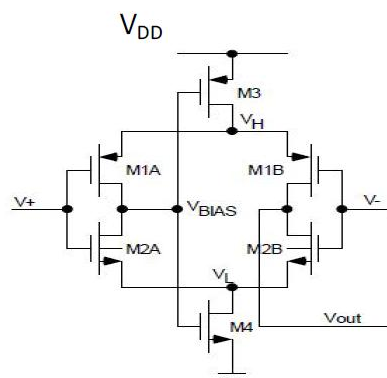


Figure 4. Post-Amplifier/Output-Buffer / Load [3]

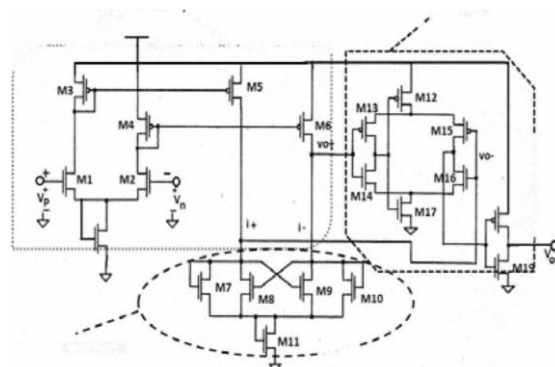


Figure 5. Preamplifier based comparator [3]

B. Preamplifier dynamic latch comparator:

Fig. 6 shows the dynamic latch comparator with preamplifier when the clock signal en goes high the comparator enters the reset phase. The comparator is resetting through the shorted transistor M13 between the two cross coupled inverters. When en goes low the circuit enters the comparison phase. Transistor M8 is connected to the voltage supply and M4 is connected to ground. The transmission close and the comparator enter the regenerative phase.

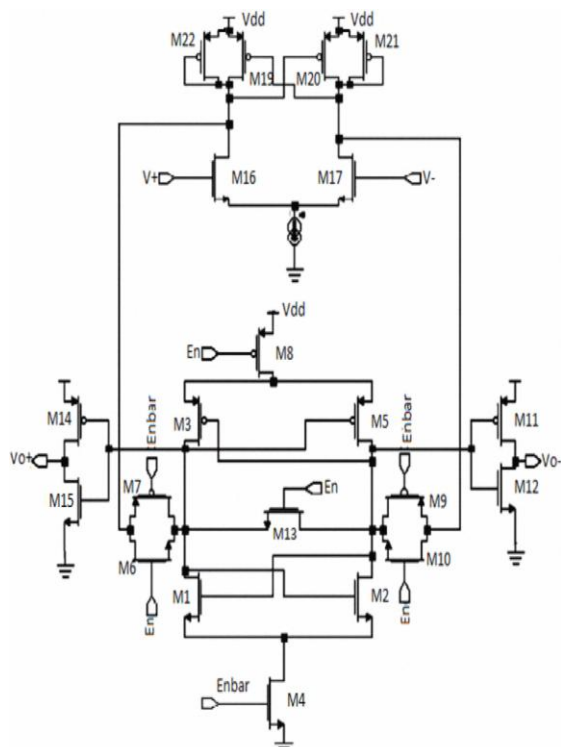


Figure 6. Preamplifier dynamic latch comparator [12]

C. Dynamic Latch Comparator With Inverter Buffer:

The schematic of the dynamic latch comparator [3] is shown in Figure 7. The transistors M1, M9 and M2, M7 form the pair of inverters and their outputs are connected to the inputs of the other. When the latch signal Lth is low and the transistors M5 and M8 are off M1, M2 are separated from M9 and M7 and the output node is pre charged to digital "1" by the transistors M3 and M4 when the latch signal Lth is high. The transistors M5 and M8 are on and the drain voltages of M1 and M2 start dropping from the positive rail. If the input is larger than the reference, the voltage at drain of M1 will drop faster than the output node. When the input reaches vdd-vth, M2 starts turning on and triggers the regenerative feedback.

The major drawback of the dynamic latch comparator is the offset error caused by transistor mismatch [6] and unbalanced charge residues [8]. The basic principle of a dynamic latch comparator comes from its positive feedback that triggers the regenerative action. This operation becomes quite slow when the voltage is in the small signal range and a large capacitive load at the output will greatly degrade the speed.

In Figure 7 inverter buffers [9] are added to isolate the comparator output and the large load capacitance. The function of the switches used between the pair of inverters of buffers is to connect and disconnect the buffer output. The inverter buffers

are used to minimize the offset errors. The timing signals latch (Lth) and the buff (clk) signals must be designed carefully to correctly represent the relationship between input and the reference.

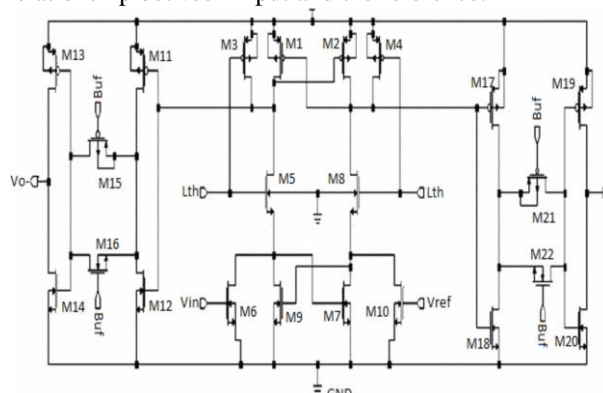


Figure 7. Dynamic latch comparator with inverter buffer [12]

IV. SIMULATION RESULTS

To compare the performance of the comparators is done and each circuit is simulated in Cadence Virtuoso Analog Design Environment. Comparison on the basis of power consumption and delay of different types of CMOS comparators at various supply voltages is done.

Table 1. Results comparison table

Comparator Name	Power dissipation (μW)	Delay (ns)
Preamplifier based comparator	81.45	0.203
Preamplifier based dynamic latch comparator	17.48	1.427
Dynamic latch comparator with inverter buffer	110.76	0.81

Figure 8 show the transient response of the preamplifier based circuit. Figure 9 and 10 show the transient response of the preamplifier dynamic latch comparator and dynamic latch comparator with inverter buffer respectively. The input and output waveforms are plotted. The inverter stage of the circuit described as final output. When the clk(en) low the output reset to vdd. When the clk is high input and reference voltage are compared and the output is obtained.

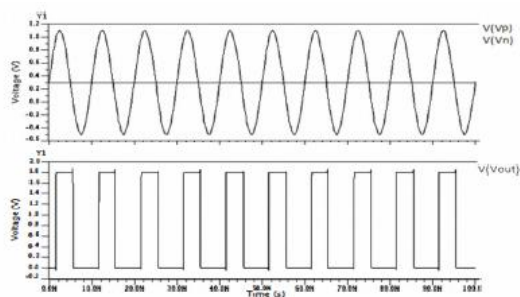


Figure8. Preamplifier based comparator

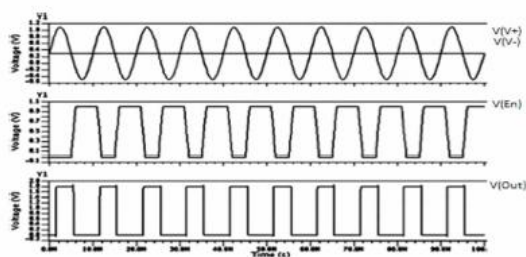


Figure 9. Preamplifier dynamic latch comparator

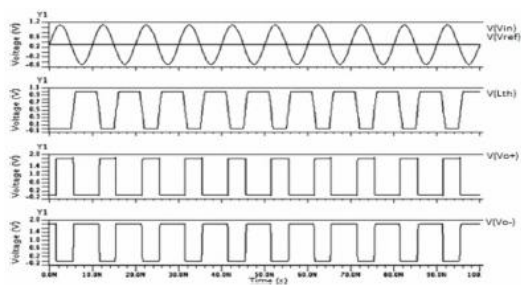


Figure 10. Dynamic latch comparator with inverter buffer

V. CONCLUSION

In this paper the power consumption & delay of different types of CMOS comparators are compared at various supply voltages. Simulation results show power consumption of the dynamic latch comparator with inverter is less compared to other type of comparators studied and 30% power reduction is obtained when compared with the conventional method.

REFERENCES

[1] Sougata Ghosh, Samraat Sharma, “Design of A Novel High Speed Dynamic Comparator with Low Power Dissipation for High Speed ADCs”, International Journal of Electronics and Computer Science Engineering, Vol. 2, Number 1, pp. 411-426.
 [2] Raghava Garipelly, “High Speed CMOS Comparator Design with 5mV Resolution” International Journal of Engineering Trends

and Technology (IJETT) – Vol. 4, Issue4- April 2013.

[3] Smriti Shubhanand, Dr. H.P. Shukla, “Design and Simulation of a High Speed CMOS Comparator”, International Journal of Electronics and Communication Engineering Vol. 6, Number 1 (2013), pp. 75-80.
 [4] Heungjun Jeon and Yong-Bin Kim, “A Novel Low-Power, Low-Offset and High-Speed CMOS Dynamic Latched Comparator”, IEEE, 2010.
 [5] Senthil Sivakumar M, Banupriya M, “High Speed Low Power Flash ADC Design for Ultra Wide Band Applications” , International Journal of Scientific & Engineering Research, Vol. 3, Issue 5, May-2012 , pp.290-295.
 [6] Miyahara, Y. Asada, P. Daehwa and A. Matsuzawa, “A Low- Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs,” in Proc. A-SSCC, Nov. 2008, pp. 269-272.
 [7] “Design of Analog CMOS Integrated Circuits”, by Behzad Razavi, Tata McGraw Hill Edition 2002, ISBN – 0-07-238032-2.
 [8] J. M. Kim, “A 6-Bit 1.3 GSAMPLE/S A/D Converter in 0.35 μ m CMOS,” Doctor Thesis, University of Texas at Dallas, Dallas, 2005.
 [9] Jun He, Sanyi Zhan, Degang Chen, and R.L. Geiger, “Analyses of Static and Dynamic Random Offset Voltages in Dynamic Comparators,” IEEE Trans. Circuits Syst. I: Reg. Papers, Vol.56, May 2009, pp. 911-919.
 [10] Bang-Sup Song, Seung-Hoon Lee and Michael F. Tempsett “A 10-b 15- MHz CMOS Recycling Two-step A/D Converter” IEEE Journal of Solid- State Circuits, vol. 25, no. 6, December 1990.
 [11] Amalan Nag, K. L. Baishnab F. A. Talukdar, Member, IEEE “Low Power, High Precision and Reduced Size CMOS Comparator for High Speed ADC Design” 2010 5th International Conference on Industrial and Information Systems, ICIIS 2010, Jul 29 - Aug 01, 2010, India.
 [12] D. lackuline Moni and P. Lisha, “High-speed and low-power dynamic latch comparator”, International Conference on Devices, Circuits and Systems (ICDCS), ICIIS 2012, March 2012, Coimbatore, India.